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82822 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of: Kozo Nakamura

Title: **SILICON CRYSTAL AND PRODUCTION METHOD FOR SILICON SINGLE CRYSTAL WAFER**

Serial No.: 09/856,209

Filed: May 18, 2001

Examiner: Matthew J. Song

Art Unit: 1765

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3/24/06 Gerard T. Shoe
Date Signature

**CORRESPONDENCE AND APPLICANT'S**
**CORRECTED BRIEF ON APPEAL UNDER 37 C.F.R. § 41.37**

Dear Sir:

Enclosed is a revised appeal brief in response to the Notification of Non-Compliant Appeal Brief (37 C.F.R. 41.37) dated February 24, 2006.

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**APPLICANT'S CORRECTED BRIEF ON APPEAL UNDER 37 C.F.R. § 41.37**

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# APPEAL BRIEF

## REAL PARTY IN INTEREST

Komatsu Denshi Kinzoku Kabushiki Kaishi, the Assignee, is the real party in interest.

## RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

## STATUS OF CLAIMS

Claims 17-20 are pending. These claims having been finally rejected are now on appeal.

Claims 1-16 were previously cancelled.

## STATUS OF AMENDMENTS

No amendments to pending claims 17-20 were filed after the date of the final rejection.

## SUMMARY OF CLAIMED SUBJECT MATTER

Claims 17 and 18 are the independent claims on appeal.

### *I. The Invention Defined By Claim 17*

As defined by claim 17, the present invention is directed to a method of producing a silicon ingot having a 60% or more GOI C mode yield and preventing the generation of dislocation clusters where $1.15 \leq (G1_{edge}/G1_{center}) \leq 1.25$ and $0.5 <$ (OSF ring inner diameter/crystal diameter) and $G1_{center}$, $G1_{edge}$ and $G2_{center}$ are temperature gradients.

$G1_{center}$ is the temperature gradient in the axial direction at the crystal center up to approximately 1350°C.

$G1_{edge}$ is the temperature gradient in the axial direction at the crystal edge up to approximately 1350°C.

$G2_{center}$ is the temperature gradient in the axial direction at the crystal center at a temperature near 1120°C.

## *I. The Invention Defined By Claim 18*

As defined by claim 18, the present invention is directed to a method of producing a silicon ingot comprising the following steps.

$G1_{edge}$, the $G1_{center}$ and the $G2_{center}$ are controlled so that both of the parameters

(1) $1.15 \leq (G1_{edge}/G1_{center}) \leq 1.25$; and

(2) $0.5 < (\text{OSF ring inner diameter/crystal diameter}) < 1.06 \times (G1_{center} \times G2_{center})^{-0.2}$ are present ($G1_{edge}$, $G1_{center}$ and $G2_{center}$ are as described in conjunction with claim 17.) and then producing a silicon single crystal ingot having 60% or more GOI C mode yield while preventing the generation of dislocation clusters.

## GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. Whether the Examiner improperly rejected claims 17-20 as unpatentable under 35 U.S.C. 103(a) over Iida et al., U.S. Patent No. 5,968,264.

## ARGUMENT

## *I. Summary of the Prior Art Applied*

Iida et al., U.S. Patent No. 5,968,264

Iida et al. teaches a method for manufacturing a silicon single crystal by the Czochralski method, in which during the growth of a silicon single crystal, the furnace temperature is controlled such that the temperature gradient difference ΔG (=Ge-Gc) is not greater than 5°C/cm, where Ge is a temperature gradient (°C./cm) at a peripheral portion of the crystal, and Gc is a temperature gradient (°C./cm) at a central portion of the crystal, both in an in-crystal descending temperature zone between 1420°C. and 1350°C. or between a melting point of silicon and 1400°C. in the vicinity of the solid-liquid interface of the crystal. In general, Ge corresponds to $G1_{edge}$ and Gc corresponds to $G1_{center}$ on the subject invention.

The Examiner has characterized Iida et al. as disclosing that wafers are sliced from a silicon ingot (col. 14, ln 20-67) and teaching that an OSF region is observed between a N region, a neutral region having few defects, and a vacancy rich region and interstitial rich region (col. 15, ln 1-15 and Fig. 10A). Further, Iida et al. teaches that $G_c$ is a temperature gradient at a central portion of the growing crystal both in an in-crystal descending zone, 1420-1350°C, or between the melting point of silicon and 1400°C in the vicinity of the solid-liquid interface of the crystal, (col. 4, ln 5-15).

## *II. The Examiner Failed to Make a Prima Facie Showing of Obviousness Based on the Iida Patent*

The Patent Office has the burden to establish a prima facie case of obviousness of the claimed subject matter as a whole within the meaning of §103. In re Fine, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988), citing, In re Piasecki, 745 F.2d 1468, 1471-72, 223 U.S.P.Q. 785, 787-88 (Fed. Cir. 1984). The burden is only satisfied by illustrating a teaching in the prior art or generally available knowledge that would lead one skilled in the art to applicant's invention as claimed. In re Lalu, 747 F.2d 703, 705, 223 U.S.P.Q. 1257, 1258 (Fed. Cir. 1984). Applicant submits that this burden has not been adequately met.

The Examiner has rejected claims 17-20, stating that Iida et al. does not teach the upper bound of $1.06x(G1_{edge}x\ G2_{center})^{-0.2}$ and that Iida et al. does teach varying the pulling rate between 1.0-0.4 mm/mind during growth of a silicon ingot and slicing wafers from the thus obtain ingot (Example 1 and Example 2). The Examiner further states that Iida et al. also shows the OSF ring diameter changes with pulling rate, such that the ratio of OSF ring diameter to crystal diameter is greater than 0.5, note Figure 10A. Therefore, the Examiner concludes that the range of OSF diameters taught by Iida et al. discloses ratios of OSF ring diameter to crystal diameter from 0.5 to about 1 and that overlapping ranges are held to be obvious (MPEP 2144.05).

In the Examiner's rationale for rejection of claims 17-20 he appears to ignore the parameter $G2_{center}$, as he must, because Iida does not teach a $G2_{center}$. As such, the Examiner's statement that Iida et al. discloses ratios of OSF ring diameter to crystal diameter from 0.5 to about 1 does not take into account the necessary element of the $G2_{center}$ and

therefore cannot be a basis for stating that there are overlapping ranges in Iida in the subject invention with regard to the parameter of $1.06x(G1_{edge}xG2_{center})^{-0.2}$. For this reason alone, the rejection should be overturned.

The Examiner has admitted that Iida does not teach the upper bound of $G2_{center}$ but argues that Figures 10A of Iida inherently encompasses the ratio range of OSF diameter. However, it should be noted that Figure 10A does not teach the first parameter set forth in claim 17, i.e., $1.15 \leq (G1_{edge}/G1_{center}) \leq 1.25$ insofar as Examples 1 and 2, which is the basis for Figures 10A and 10B, states that $\Delta G$ is 3.0°C/cm, which leads to a $G1_{edge}/G1_{center}$ outside the claimed range. Thus, Figure 10A cannot teach the invention of claim 17 nor can it lead one to the invention of claim 17.

As a result, the Examiner's reliance on Figure 10A of Iida is misplaced.

One cannot learn from the teachings of Iida et al. to produce a silicon ingot with 60% or more GOI C mode yield under the conditions set forth in claim 17. More specifically, Examples 1 and 2 of Iida et al., insofar as they are directed to silicon melts having a $\Delta G$ of 3.0°C/cm cannot be used in rendering the subject invention obvious as such does not satisfy the conditions set forth in the claims, i.e., $1.15 \leq (G1_{edge}/G1_{center}) \leq 1.25$. Thus, Iida et al.'s invention does not make the subject invention of claim 17 obvious.

As stated, claim 17 requires the production of a silicon single crystal ingot having 60% or more GOI C mode yield. GOI (Gate Oxide Integrity) is a physical parameter gained by measuring the TZDB voltage histogram by applying a step voltage to the MOS capacitors and monitoring the oxide leakage current, then determining the dielectric breakdown defect density which is caused by silicon wafers. The defect density is determined from the B-mode failure fraction. This test method characterizes the Si wafer and is very useful in the crystal defect (mainly COP) evaluation of a mirror polished wafer.

GOI C Mode yield refers to a method of characterizing breakdown failure results, which can be summarized in terms of ranges of oxide electric field in which the breakdown occurred. One set of categories (A, B and C for TZDB ) widely used is as follows:

A mode failure: $0 \text{ MV/cm} \leq Ebd < 3 \text{ MV/cm}$

B mode failure: $3 \text{ MV/cm} \leq Ebd < 8 \text{ MV/cm}$

C mode failure: $8 \text{ MV/cm} \leq Ebd$

The A mode failure is generally an initial short and is caused by pinholes of oxide films

formed in the gate oxide process. The COP does not cause these oxide pinholes. The B mode failure is generally an accidental breakdown. The COP is main origin of a B mode failure. The C mode failure (which is concerned here) is related to fatigue breakdown. The failure mode is partly caused by COP, but is almost always caused by extensive wear.

In the subject specification, it is stated that "if the C mode yield for the GOI is 60% or higher, the crystal can be regarded as better than crystals normally in use." (see Page 16, line 2 from the bottom).

Applicant has made the discovery that the failure rate decreases when the GOI C Mode yield is 60% or higher. Iida makes no mention or suggestion that such a parameter is to be taken into consideration.

The Examiner also notes Figure 8 of Iida et al., which states that $\Delta G$ is 5°C/mm. The applicant notes that the $\Delta G$ units of Figure 8 is measured in time (°C/min) and not distance (°C/cm) as discussed in connection with Figure 10A and Example 1, and thus at that point Figure 8 is not directly comparable to the other examples of Iida et al. or the temperature gradients recited by the subject claims 17 and 18, without considering the temperature gradient specified for the subject invention, i.e., °C/mm (see pages 7 and 8 of the specification). As a result, Figure 8 cannot be utilized in rendering the subject claims obvious.

Claim 18 is directed to a method of producing a silicon ingot, which comprises the steps of controlling the specific temperature gradients of the ingot so that the two equations set forth are followed. As set forth above, Iida cannot make obvious claim 18 in that the first parameter i.e., $1.15 \leq (G1_{edge}/G1_{center})$ is $\leq 1.25$ is not satisfied by Figures 8, 10A or Examples 1 and 2, and further the second parameter $G2_{center}$ is not envisioned or even suggested in Iida. As a result, neither of these two parameters is fulfilled and thus, claim 18 cannot be made obvious by the invention of Iida et al.

## CONCLUSION

In conclusion, Applicant submits those claims 17-20 presently pending and on appeal are allowable over the art of record because the Examiner has failed to make a prima facie showing that the claims would have been obvious to one of skill in the art

over the art of record. To this end, Applicant respectfully requests that the Board reverse the decision of the Examiner finally rejecting Claims 17-20.

Respectfully submitted,

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## APPENDICES

## I. CLAIMS ON APPEAL

17. A method of producing a silicon ingot, comprising:

producing a silicon single crystal ingot having 60% or more GOI C mode yield and being prevented from generation of dislocation clusters under the following conditions:

(1) $1.15 \leq (G1_{edge}/G1_{center}) \leq 1.25$;

(2) $0.5 < (\text{OSF ring inner diameter/crystal diameter}) < 1.06 \times (G1_{center} \times G2_{center})^{-0.2}$ where

$G1_{center}$ is a temperature gradient in the axial direction at the crystal center in the temperature region from the solid-liquid interface temperature to approximately 1350°C, $G1_{edge}$ is a temperature gradient in the axial direction at the crystal edge in the temperature region from the solid-liquid interface temperature to approximately 1350°C, $G2_{center}$ is a temperature gradient in the axial direction at the crystal center near 1120°C.

18. A method of producing a silicon ingot, comprising the steps of:

controlling the $G1_{edge}$, the $G1_{center}$ and the $G2_{center}$ of the ingot so that:

(1) $1.15 \leq (G1_{edge}/G1_{center}) \leq 1.25$;

(2) $0.5 < (\text{OSF ring inner diameter/crystal diameter}) < 1.06 \times (G1_{center} \times G2_{center})^{-0.2}$ where

$G1_{center}$ is a temperature gradient in the axial direction at the crystal center in the temperature region from the solid-liquid interface temperature to approximately 1350°C, $G1_{edge}$ is a temperature gradient in the axial direction at the crystal edge in the temperature region from the solid-liquid interface temperature to approximately 1350°C, and $G2_{center}$ is a temperature gradient in the axial direction at the crystal center near

1120°C; and

producing a silicon single crystal ingot having 60% or more of GOI C mode yield and being prevented from generation of dislocation clusters.

19. A method of producing a silicon wafer comprising:

cutting the wafer from portions, of the ingot of claim 18, in which the inner diameter of the OSF ring is at least 1/2 the crystal diameter.

20. A method of producing a silicon wafer comprising:

cutting the wafer from portions, of the ingot of claim 19, in which the inner diameter of the OSF ring is at least 1/2 the crystal diameter.

## II. EVIDENCE

None

## III. RELATED PROCEEDINGS

None

## IV. TABLE OF AUTHORITIES

In re Fine, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988).

In re Piasecki, 745 F.2d 1468, 1471-72, 223 U.S.P.Q. 785, 787-88 (Fed. Cir. 1984).

In re Lalu, 747 F.2d 703, 705, 223 U.S.P.Q. 1257, 1258 (Fed. Cir. 1984).